# Electrical Data

For Electrical Data See Document "Nx586 Electrical Specifications"
Order # NxDOC-ES001-01-W

THIS PAGE INTENTIONALLY LEFT BLANK

# Mechanical Data

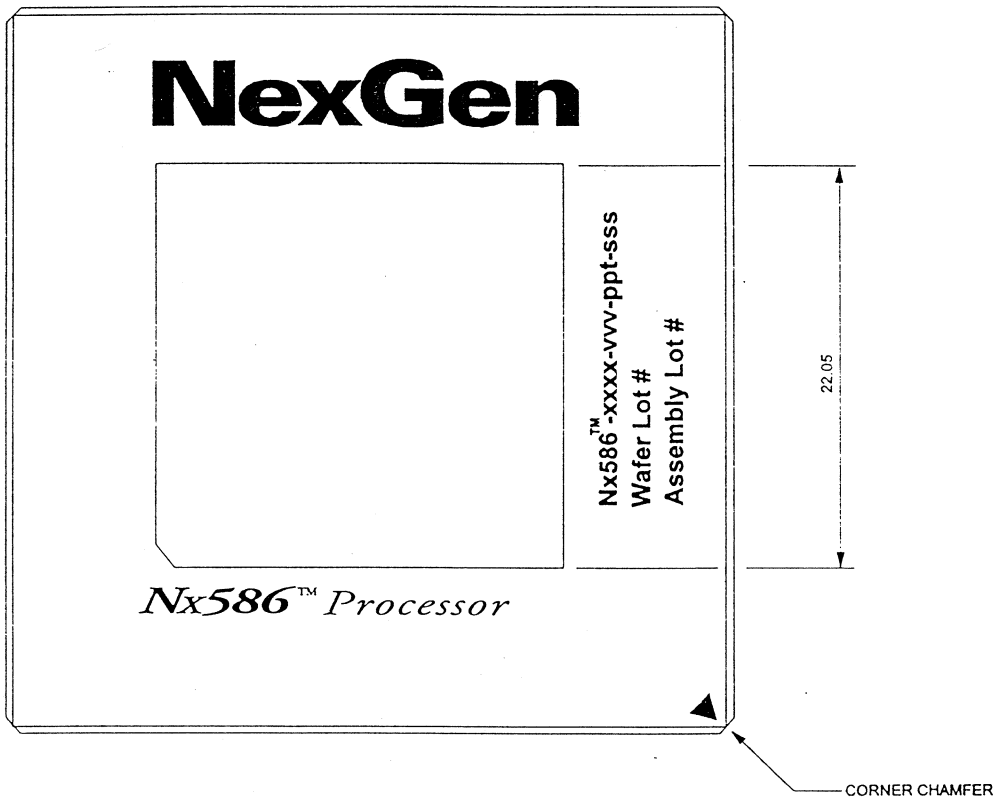


Figure 42 Nx586 Package Diagram (top)

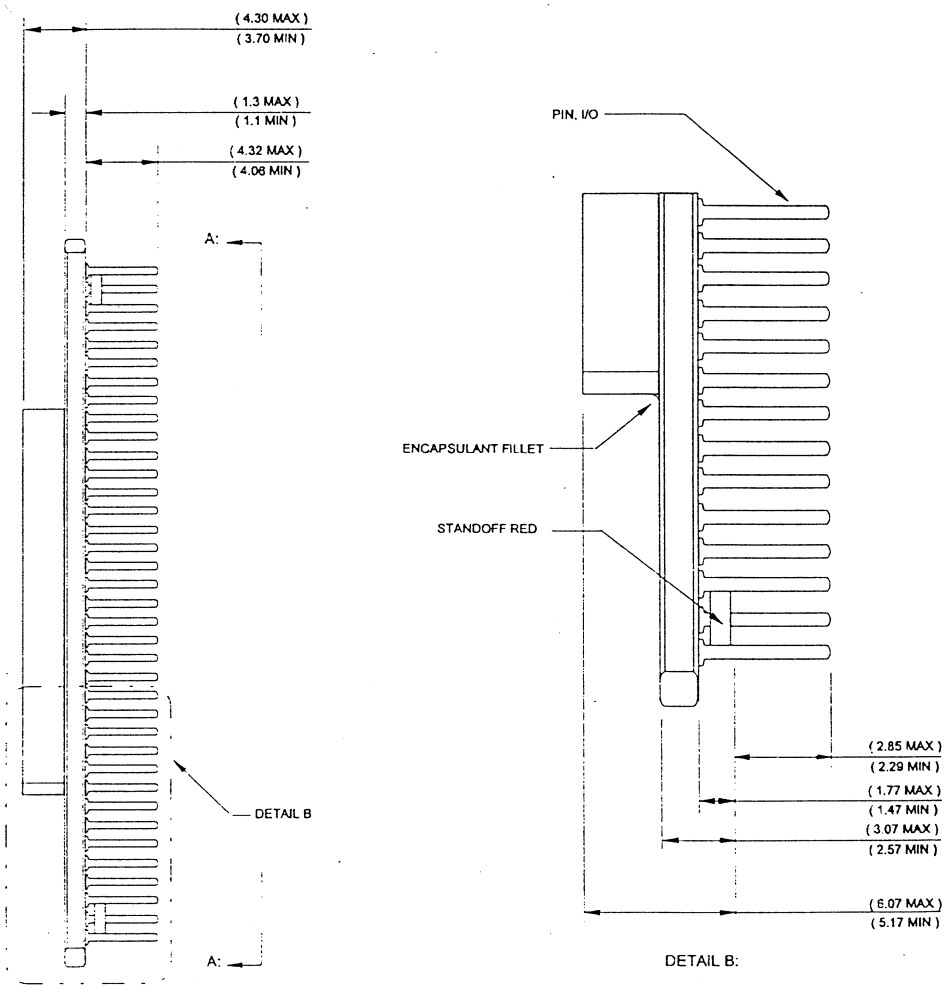


Figure 43 Nx586 Package Diagram (side)

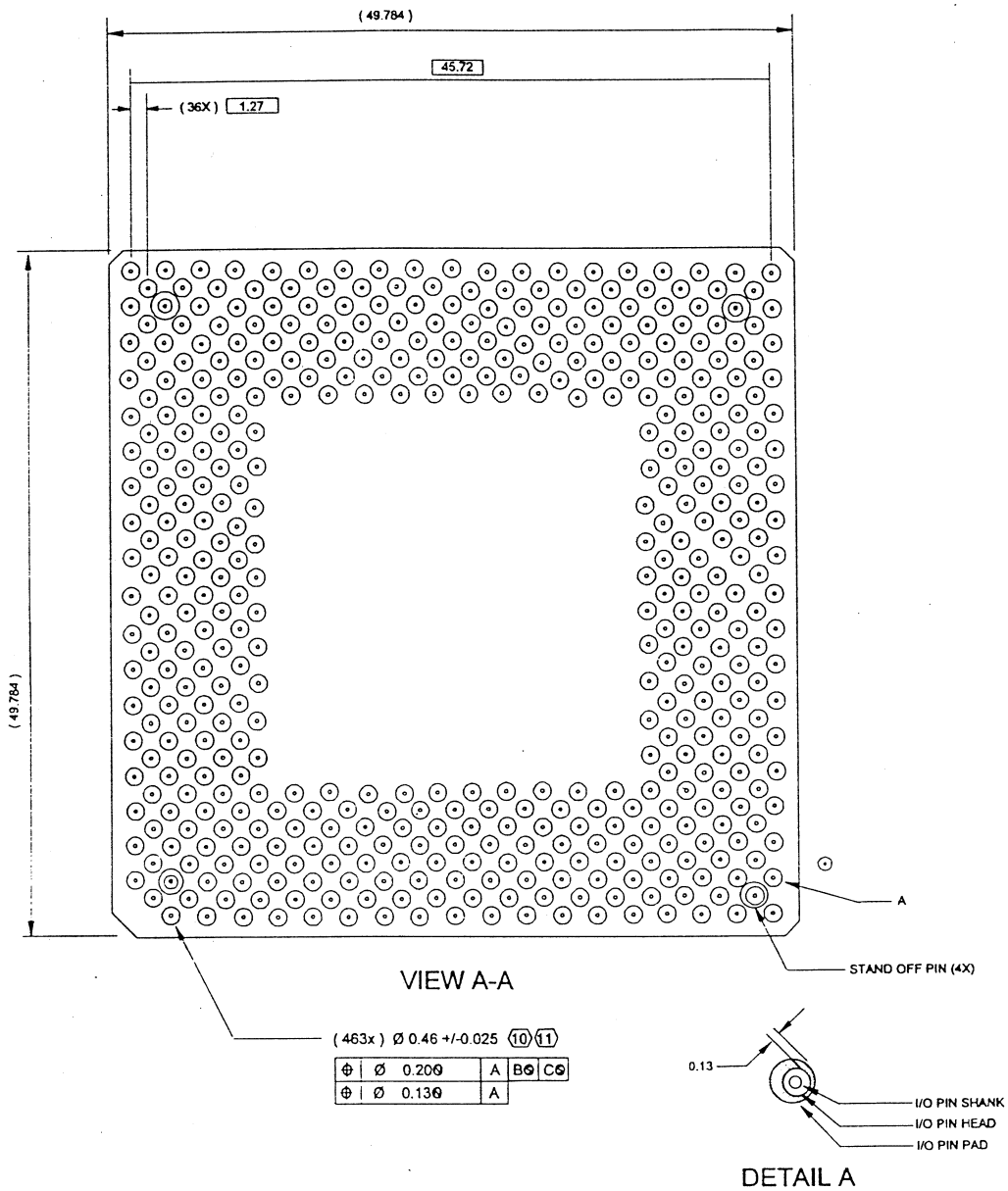


Figure 44 Nx586 Package Diagram (bottom)

# Glossary

Access—A bus master is said to "have access to a bus" when it can initiate a *bus cycle* on that bus. Compare *bus ownership*.

Adapter—A central processor, memory subsystem, I/O device, or other device that is attached to a slot on the NexBus, VL-Bus, or ISA bus. Also called a *slot*.

Aligned—Data or instructions that have been rotated until the relevant bytes begin in the least-significant byte position.

Allocating Write—A read-to-own (read for exclusive ownership of cacheable data) followed by a write to the cache.

Arbiter—A resource-conflict resolver, such as the NexBus arbiter.

Asserted—For signals, "asserted" means driven to the state which asserts the description of the signal.

Active High—The signal or memory bit drive to its "asserted" state which is logically or physically high. For a memory bit, this would be a "1". For a signal, this would be near VCC voltage level.

Active Low—The signal or memory bit drive to its "asserted" state which is logically or physically low. For a memory bit, this would be a "0". For a signal, this would be near GND voltage level.

b—Bit.

B—Byte.

Bandwidth—The number of bits per second that can be processed by a memory, arithmetic unit, input/output processor, or communication system.

Bank—In a cache, same as *set* and *way*. In main memory, a qword-wide group of addressable locations.

Branch Prediction—The use of history, statistical methods, or heuristic rules to predict the outcome of conditional branches.

Buffer—A fraction of real memory or a group of registers that serve as a buffer for data flowing to and from auxiliary memory.

Bus Cycle—A complete transaction between a bus master and a slave. For the Nx586 processor, a bus cycle is typically composed of an address and status phase, a data phase, and any necessary idle phases. Also called a *bus operation*, or simply *operation*.

Bus Operation—Same as *bus cycle.*

Bus Ownership—A bus is said to be owned by a master when the master can initiate cycles on the bus. The master to which bus ownership is granted controls only its own interface with the arbiter. The arbiter, on behalf of that master, acts as a master on the other buses in the system. It does this so as to support the master in the event that a bus-crossing operation is requested. Compare *access.*

Bus Phase—Part of bus cycle that lasts one or more bus clocks. For example, it may be a transfer of address and status, a transfer of data, or idle clocks.

Bus Sequence—A sequence of bus cycles (or operations) that must occur sequentially due to their being explicitly locked by the continuous assertion of the master's AREQ* and/or LOCK* signals, or implicitly locked by the GDCL signal.

Cache Block—A 32-byte unit of data in a cache. The Nx586 processor's caches are organized around such blocks. Each cache block has an associated tag and MESI-protocol state. Cache blocks can be fetched atomically as a contiguous group of 32-bytes or in eight-byte subblock units. Compare *cache line.*

Cache-Block Tag—The high-order address bits of a cache block that identifies the area of memory from which it was copied. During a cache lookup, the high-order address bits of the processor's operand is compared with the tags of all blocks stored in the cache.

Cache Coherence—The protocol among multiprocessors with private caches that assures that each variable in the shared memory space receives writes in a serial order, and no processor sees that sequence of values in any other order.

Cache Hit—An access to a cache block whose state is *modified, exclusive,* or *shared* (i.e., not *invalid).* Compare *cache miss.*

Cache Line—If a *cache block* can be fetched atomically (rather than in subblock units), the concepts of cache block and cache line are identical. However, in the Nx586 processor, cache blocks are often fetched in eight-byte subblock units, leaving only parts of the cache block valid. Compare *cache block.*

Cache Lookup—Comparison between a processor address and the cache tags and state bits in all four sets (ways) of a cache.

Cache Miss—An access to a cache block whose state is *invalid.* Compare *cache hit.*

Caching Master—A bus master that internally caches data originated elsewhere. The caching master must continually monitor the bus to guarantee cache coherency. Masters on buses other than the NexBus can maintain caches, but they must be write-through (not write-back) caches.

Conditional Branch—A computer instruction that alters the sequence of execution if a condition is true, and otherwise falls through to the next instruction in sequence.

Clean—Same as *exclusive.*

Clock Cycle—Unless otherwise stated, this a *processor-clock cycle* rather than a bus-clock cycle. The Nx586 processor's clock runs at twice the frequency of the NexBus clock (NxCLK). The level-1 cache runs at the same frequency as the processor clock. The level-2 cache runs at the same frequency as the NexBus clock (NxCLK).

Clock Phase—One-half of a processor clock cycle.

Cycle—See *bus cycle*, *clock cycle*, *bus phase*, and *clock phase*.

D Cache—The level-1 (L1) data cache.

Device—Same as *adapter*.

Dirty—Same as *modified*.

Dword—A doubleword. A four-byte (32-bit) unit of data that is addressed on an four-byte boundary. Also called a *dword* (doubleword).

Exclusive—One of the four states that a 32-byte cache block can have in the MESI cache-coherency protocol. *Exclusive* data is owned by a single caching device and is the only known-correct copy of data in the system. Also called *clean* data. When exclusive data is written over, it is called *modified* (or *dirty)* data.

Floating Point Execution Unit—The Floating Point Execution Unit. The logic in the Floating Point Execution unit is integrated into the parallel pipeline of the Nx586 processor.

Flush—(1) To write back a cache block to memory and invalidate the cache location, also called *write-back and invalidate*, or (2) to invalidate a storage location such as a register without writing the contents to any other location. This is an ambiguous term that is best not used.

Functional Unit—The Decode Unit, Address Unit, Integer Unit, Floating Point Coprocessor, or Cache and Memory Unit.

Group Signal—A NexBus control signal that represents the logical OR of several inputs. These signals typically have signal names that begin with the letter "G".

I Cache—The level-1 (L1) instruction cache.

Invalid—One of the four states that a 32-byte cache block can have in the MESI cache-coherency protocol. *Invalid* data is not correctly associated with the tag for its cache block.

Invalidate—To change the state of a cache block to *invalid*.

L1 or Level-1—The level-1 or primary cache is located on the Nx586 processor chip.

L2 or Level 2—The level-2 or secondary cache is located in SRAM connected to the processor's SRAM bus and controlled by logic on the Nx586 processor.

Line—See *cache block*.

Main Memory—See *memory*.

Master—The Master is a device on the NexBus that initiates a transaction.

Memory—A RAM or ROM subsystem located on any bus, including the *main memory* most directly accessible to a processor. Also called *main memory*.

MESI—The cache-coherency protocol used in the Nx586 processor. In the protocol, cached blocks in the L2 write-back cache can have four states (modified, exclusive, shared, invalid), hence the acronym MESI. See *modified*, *exclusive*, *shared*, and *invalid*.

Modified Write-Once Protocol—The cache-coherency protocol used in the Nx586 processor. See *MESI*.

Modified—One of the four states that a 32-byte cache block can have in the MESI cache-coherency protocol. *Modified* data is *exclusive* data that has been written to after being read from lower-level memory, and is therefore the only valid copy of that data. Also called *dirty or stale.*

MWO—See *modified write-once protocol.*

NB—Same as *NexBus.*

Negated— For signals, "negated" means driven to the state which de-asserts the description of the signal. Or the opposite of "asserted".

NexBus—A 64-bit synchronous, multiplexed bus defined by NexGen.

No-Op—A single-qword operation with BE<7:0>* all negated. No-ops address no bytes and do nothing except consume processor cycles.

Nx586—The Nx586 processor (CPU).

NxVL—A NexBus system controller chip that supports a Nx586 processor, main memory, 82C206 peripheral controller, VL-Bus, and ISA bus.

Octet—A unit of data consisting of eight bytes and addressed on an eight-byte boundary.

Operation—See *bus operation.*

Owned—A cache block whose state is *exclusive* (owned clean) or *modified* (owned dirty). See also *bus ownership.*

Ownership—See *bus ownership.*

Peripheral Controller—A chip that supports interrupts, DMA, timer/counters, and a real-time clock.

Phase—See *bus phase* and *clock phase.*

PLL—Phase-locked loop.

POST—Power On Self Test. This procedure is performed when power is first applied to check the functionality of the system..

Present—Same as *valid.*

Processor—Unless otherwise specified, refers to a Nx586 processor.

Processor Clock—The Nx586 processor clock. See *clock cycle.*

Qword—A quadword. A eight-byte unit of data that is addressed on an eight-byte boundary.

Register Renaming—A technique used in processor design that assigns idle registers to serve in the place of program specified registers in order to avoid conflicts that could stall pipeline flow momentarily.

RISC—Reduced Instruction-Set Computer. A computer in which all instructions are simple instructions that take one cycle to execute, except possibly for delays introduced by conditional branches and cache misses.

Scalar Operation—Any operation performed on individual data.

Scalar Processor—A processor whose basic operations manipulate individual data elements rather than vectors or matrices.

Set—In a cache, one of the degrees of associativity. The group of cache blocks in such a set. Same as *bank* and *way*.

Shared—One of the four states that a 32-byte cache block can have in the MESI cache-coherency protocol. *Shared* data is valid data that can only be read, not written.

Snoop—To compare an address on a bus with a tag in a cache, so as to detect operations that are inconsistent with cache coherency.

Snoop Hit—A snoop in which the compared data is found to be in a *modified* state. Compare *snoop miss*.

Snoop Miss—A snoop in which the compared data is not found, or is found to be in a *shared* state. Compare *snoop hit*.

Source—In timing diagrams, the left-hand column of the diagram indicates the "source" of each signal. This is the chip that originated the signal as an output. When signals are driven by multiple sources, all sources are shown, in the order in which they drive the signal. The source of a signal that takes on a different name as it crosses buses through transceivers is shown as the transceivers overwhich the signals cross, subscripted with a symbol indicating the logic that originally output the signals. The source of group-ORed signals (such as GXACK) is likewise subscripted with a symbol indicating the logic that originally output the activating signal (such as XACK*).

Stale—Same as *modified*.

System Bus—A bus to which the NexBus interfaces. The system buses include the VL-Bus, PCI-Bus and ISA bus.

System Controller—The device or logic that provides NexBus arbitration and interfacing to main memory and any other buses in the system.

Superscalar—A computer architecture in which multiple scalar instructions are decode in each clock cycle sot that the instruction completed per cycle exceeds 1.0.

T-Byte—An 80-bit floating-point number.

Word—A two-byte (16-bit) unit of data.

Write-Back Cache—A cache in which WRITEs to memory are stored in cache and written to memory only when a rewritten item is removed from cache.

Write-Through Cache—A cache in which WRITEs to memory are recorded concurrently both in cache and in main memory. The result is that the main memory slways contains valid data

THIS PAGE INTENTIONALLY LEFT BLANK

# Index

NexGen

1623 Buckeye Drive
Milpitas, CA 95035
Ph 1-800-8NEXGEN
Fax (408) 435-0262

18 bis rue du montceau
77133 Féricy (France)
Ph 33 (1) 64.23.68.65
Fax 33 (1) 64.23.61.91